WHAT IS CLAIMED IS:

1. A tuner block:

a tuner which tunes a broadcasting signal;

an IF/demodulator circuit which demodulates the broadcasting signal tuned by the tuner;

a modulator which modulates an input video signal and an input audio signal into an RF signal;

a casing which accommodates the tuner, the IF/demodulator circuit and the modulator; and

a plurality of pins disposed consecutively on an outer side of the casing, the plurality of pins to input and/or output signals and a voltage to operate the tuner, the IF/demodulator circuit and the modulator;

wherein one of the plurality of pins is a power supply pin through which an electrical power is supplied from an outside power supply, and the tuner and the modulator are connected commonly to the power supply pin inside of the casing.

2. The tuner block according to claim 1, wherein, among the plurality of pins, a first pin through a fifth pin are used by the modulator, a sixth pin through an eleventh pin and a fourteenth pin are used by the tuner, and a twelfth pin, a thirteenth pin and a sixteenth pin are used by the IF/demodulator circuit.

3. The tuner block according to claim 2, wherein, among the plurality of pins, a fifteenth pin is a reserved pin which is not used.

4. The tuner block according to claim 3, wherein, among the plurality of pins, the third pin is the power supply pin.

5. The tuner block according to claim 4, wherein, among the plurality of pins, a seventh pin is a clock input pin which inputs a clock signal for use in the modulator and the tuner.

6. The tuner block according to claim 5, wherein, among the plurality of pins,

the first pin is an audio input pin which inputs an audio signal transmitted from an audio/video block,

the second pin is a channel selection pin which inputs a channel selection signal which selects an output channel of the modulator,

the forth pin is a control pin which inputs a control signal to convert between a TV mode and a VCR mode, and

the fifth pin is a video input pin which inputs the input video signal.

7. The tuner block according to claim 6, wherein, among the plurality of pins,

the sixth pin is an automatic gain control pin which controls a gain of the broadcasting signal tuned by the tuner,

the eighth pin is an AS pin which inputs a signal to select one of the tuner and at least one other tuner,

the ninth pin is an SCL pin which inputs another clock signal used to communicate with a CPU,

the tenth pin is an SDA pin which inputs a command transmitted from the CPU,

the eleventh pin is an AFT pin which outputs a reference voltage to the CPU, to enable an automatic fine tuning, and

the fourteenth pin is a TU-V pin which outputs another reference voltage used to determine local oscillation of a frequency required by a selected channel.

8. The tuner block according to claim 7, wherein, among the plurality of pins,

the twelfth pin is an audio output pin which outputs an audio signal demodulated by the IF/demodulator circuit,

the thirteenth pin is an SIF output pin which outputs a sound sub-carrier, and

the sixteenth pin is a video output pin which outputs a video signal demodulated by the IF/demodulator circuit.

9. A tuner block comprising:

a tuner which tunes a broadcasting signal;

an IF/demodulator circuit which demodulates the broadcasting signal tuned by the tuner;

a modulator which modulates an input video signal and an input audio signal into an RF signal;

a casing which accommodates the tuner, the IF/demodulator circuit and the modulator; and

a plurality of pins disposed consecutively at intervals on an outer side of the casing, the plurality of pins to input and/or output signals and a voltage to operate the tuner, the IF/demodulator circuit and the modulator;

wherein the plurality of pins comprises,

an audio output pin which outputs an audio signal demodulated by the IF/demodulator circuit,

a video output pin which outputs a video signal demodulated by the IF/demodulator circuit, wherein the video output pin is distanced from the audio output pin by at least four pin intervals,

an SIF output pin disposed adjacent to the audio output pin, the SIF output pin to output a sound sub-carrier, and

a clock input pin distanced from the SIF output pin by at least six pin intervals, the clock input pin to input a clock signal to the modulator and the tuner.

10. The tuner block according to claim 9, wherein the SIF output pin is disposed between the audio output pin and the video output pin.

11. The tuner block according to claim 10, wherein:

a TU-V pin which outputs a reference voltage used to determine local oscillation of a frequency required by a selected channel, and a reserved pin which is not used, are disposed between the SIF output pin and the video output pin.

12. The tuner block according to claim 11, wherein:

a total number of the plurality of pins is sixteen,

the audio output pin, the SIF output pin, the TU-V pin, the reserved pin and the video output pin are a twelfth pin through a sixteenth pin, respectively, among the sixteen pins, and

the clock input pin is a seventh pin among the sixteen pins.

13. The tuner block according to claim 12, wherein:

among the sixteen pins, a first pin through a fifth pin are used by the modulator, and a sixth pin through an eighth pin and an eleventh pin are used by the tuner.

14. The tuner block according to claim 13, wherein:

the first pin through the fifth pin are, respectively,

an audio input pin which inputs the input audio signal,

a channel selection pin which inputs a channel selection signal to select an output channel of the modulator,

a power supply pin which supplies electrical power to the modulator and the tuner,

a control pin which inputs a control signal to convert between a TV mode and a VCR mode, and

a video input pin which inputs the input video signal.

15. The tuner block according to claim 14, wherein,

the sixth pin is an automatic gain control pin which controls a gain of the broadcasting signal tuned by the tuner, and

the eighth pin through the eleventh pin are, respectively, an AS pin which inputs a signal to select one of the tuner and at least one other tuner, an SCL pin which inputs another clock signal used to communicate with a CPU, an SDA pin which inputs a command transmitted from the CPU, and an AFT pin which outputs another reference voltage to the CPU, to enable an automatic fine tuning.

16. A tuner block comprising:

a tuner which tunes a broadcasting signal;

an IF/demodulator circuit which demodulates the broadcasting signal tuned by the tuner;

a modulator which modulates an input video signal and an input audio signal into an RF signal; and

sixteen pins disposed consecutively on an outer side of the casing, the pins to input and/or output signals and a voltage needed to operate the tuner, the IF circuit and the modulator; wherein:

a first pin inputs the input audio signal,

a second pin inputs a channel selection signal to select an output channel of the modulator,

a third pin inputs the voltage to the modulator and the tuner,

a fourth pin inputs a control signal to convert between a TV mode and a VCR mode,

a fifth pin inputs the input video signal;

a sixth pin inputs a signal to control a gain of the broadcasting signal tuned by the tuner,

a seventh pin inputs a clock signal to the modulator and the tuner,

an eighth pin inputs an AS signal to select one of the tuner and at least one other tuner,

a ninth pin inputs another clock signal used to communicate with a CPU,

a tenth pin inputs a command transmitted from the CPU,

an eleventh pin outputs a reference voltage to the CPU, to enable automatic fine tuning,

a twelfth pin outputs an output audio signal demodulated by the IF/demodulator circuit,

a thirteenth pin outputs a sound sub-carrier,

a fourteenth pin outputs another reference voltage to determine local oscillation of a frequency required by the selected channel,

a fifteenth pin is a reserved pin which is not used, and

a sixteenth pin outputs an output video signal demodulated by the IF/demodulator circuit.

17. An interface circuit for selectively using one of a first tuner block having a first predetermined number of connector pins and a second tuner block having a second predetermined number of connector pins, wherein a third predetermined number of corresponding pins of the first and second predetermined numbers of pins have different functional assignments, the interface circuit comprising:

a first switch which connects a first of the corresponding pins to a power supply input voltage to selectively use the first tuner block or connects the first corresponding pin to an audio output function to selectively use the second tuner block;

a second switch which disconnects a clock input signal from a second of the corresponding pins to selectively use the first tuner block and connects the clock input signal to the second corresponding pin to selectively use the second tuner block;

a third switch which connects the clock input signal to a third of the corresponding pins to selectively use the first tuner block and disconnects the clock input signal from the third corresponding pin to selectively use the second tuner block;

a fourth switch which connects the third corresponding pin to a sound sub-carrier output to selectively use the second tuner block and disconnects the third corresponding pin from the sound sub-carrier output to selective use the first tuner block;

a fifth switch which disconnects an automatic fine tuning output from a fourth of the corresponding pins to selectively use the first tuner block and connects the fourth corresponding pin to the automatic fine tuning output to selectively use the second tuner block; and

a sixth switch which connects a video output to a fifth of the corresponding pins to selectively use the second tuner block and disconnects the fifth corresponding pin from the video output to selectively use the first tuner block.

18. An interface circuit for selectively using one of a first tuner block having a first predetermined number of connector pins and a second tuner block having a second predetermined number of connector pins, wherein a third predetermined number of corresponding pins of the first and second predetermined numbers of pins have different functional assignments, the interface circuit comprising:

a circuit board having a plurality of circuit paths, each circuit path connecting a respective pin of the third predetermined number of corresponding pins with additional circuitry, each of the plurality of circuits path having an opening in the circuit path adapted to receive a jumper;

a first jumper which completes a first of the plurality of circuit paths to connect a first of the corresponding pins to a power supply input to selectively use the first tuner block or completes a second of the plurality of circuit paths to connect the first corresponding pin to an audio output to selectively use the second tuner block; and

a second jumper which completes a third of the plurality of circuit paths to connect a clock input to a second of the corresponding pins to selectively use the second tuner block or completes a fourth of the plurality of circuit paths to connect the clock input to a third of the corresponding pins to selectively use the first tuner block.

19. The interface circuit according to claim 14, further comprising:

a third jumper which completes a fifth of the plurality of circuit paths to connect the third corresponding pin to a sound sub-carrier output to selectively use the second tuner block;

a fourth jumper which completes a sixth of the plurality of circuit paths to connect a fourth of the corresponding pins to an automatic fine tuning output to selectively use the second tuner block; and

a fifth jumper which completes a seventh of the plurality of circuit paths to connect a video output to a fifth of the corresponding pins to selectively use the second tuner block.